Circuit Seed™ Track & Hold Design for License

Phase noise describes the stability in the frequency domain while jitter describes the stability in the time domain. RF (Radio Frequency) engineers working in radar and base station design will be interested in phase noise since poor phase noise performance will affect up/down conversions and channel spacing. Digital engineers working in Time Division Multiplexing (telecom infrastructure) will be interested in jitter since poor jitter performance will result in network slips and excessive re-send traffic. As is well known, jitter is a dominant limiting parameter in QAM and other ADC signal processing procedures.

The measure of performance for a S/H system operating in a charge mode, the process is to accurately freeze and isolate an input voltage as charge **Qs** on a sampling capacitor, which is cutoff at a precisely defined point in time, independent of signal amplitude and frequency content, and present this captured charge as a buffered voltage for subsequent analog signal processing. This capacitor is a flying capacitor with capacitively symmetrical transmission-gate switches preferably on both ends of the capacitance. The sampling capacitor needs to be a cordwood or fringe capacitor made out of IC interconnect wiring and the insulation between interconnect. The value of this native capacitance has a very low dependency on the charge it holds. Although not necessary due to the low typical capacitor value of ~1pf, IC process extension high-k MIM capacitors can be used if their capacitance does not vary with stored voltage. Jitter-free samples, independent of their signal amplitude, are required for QAM and other DSP signal processing.

The combination between series and parallel of multiple sampling capacitors can provide precise analog mathematical operations on sampled voltages. For instance, separate sampled analog voltages can be rearranged in series to double their subsequent presented value. Multiple samples of the same voltage can be integer multiplied when rearranged in series or in parallel around an OpAmp – ideal for an ADC or DAC. Offset voltage and noise can be down-sampled out of the operating signal frequencies.

This voltage manipulation methodology can be implemented with capacitors that use only interconnect metal and the insulator between them. It is available in any IC process including nanoscale process nodes as they are introduced. Generic cordwood or MIM (Metal-Insulator-Metal) interconnect capacitors possess the highest quality of any capacitor and scale nicely down into nanoscale IC process nodes. In addition to the generic interconnect wiring insulator, a high-k dielectric option is often available early on as process nodes incorporate process extensions, making these MIM capacitors more compact. Nanoscale gate oxides are a high-k dielectric, pointing to MIM high-k option inclusion.

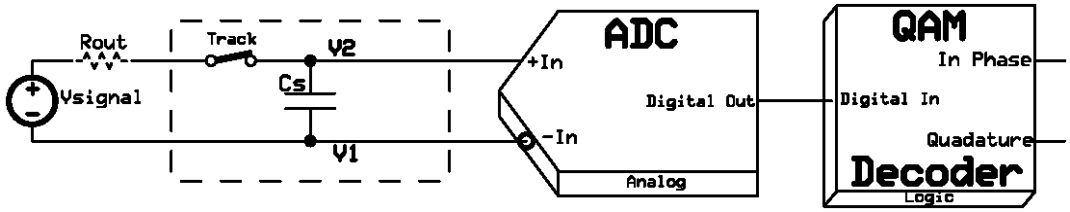

Figure **1** – *Example Track & Hold application*

Track & Hold circuits freeze their varying analog input voltage at a precisely logically defined time and hold the sample long enough to be digitized by an ADC for further digital signal processing.

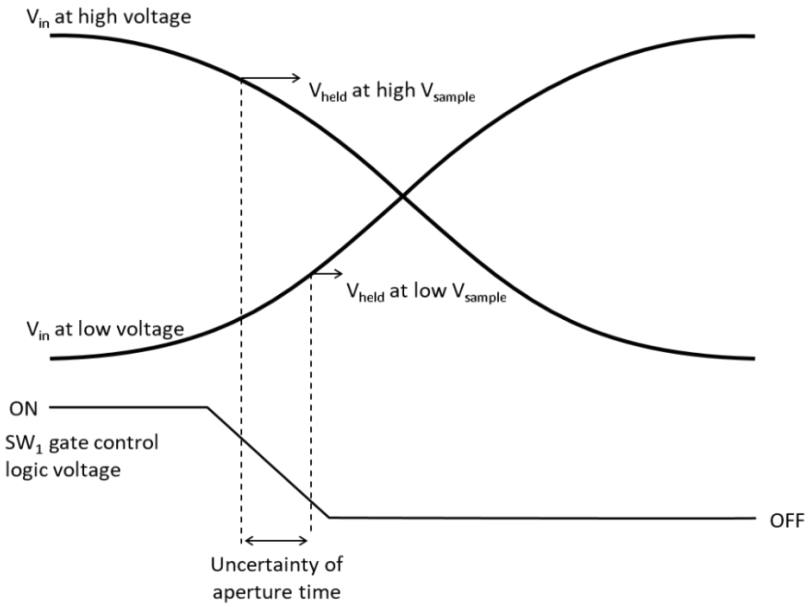

Figure **2.1** – *Aperture time dependence on sampled signal voltage*

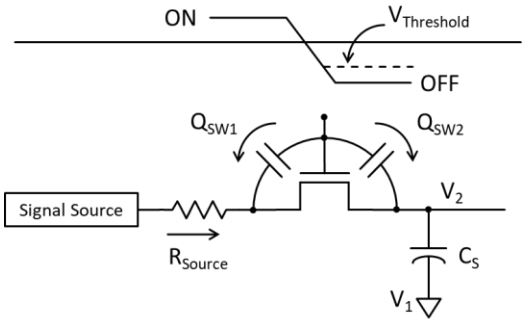

Figure **2.2** – *MOSFET switch charge transfer capacitances at turnoff*

The tracking switch turns off when its MOS gate voltage is a threshold away from the channel voltage. When channel voltage is high, the sample aperture time is different from when the channel voltage is low causing an uncertainty in aperture time seen as sampling jitter or phase noise. The solution was mitigated by switching the gate as fast as possible to shorten the range of uncertainty.

The purpose of the Circuit Seed Track & Hold is to freeze and isolate an input voltage as charge (Q=CV) on a sampling capacitor at a precisely defined point in time, independent of signal amplitude and frequency content, which up to now has impacted that precision. This captured charge serves as an instantaneous battery of voltage (V = Q/C) for subsequent signal processing. This type of tracking capacitor is often called a flying capacitor because both sides can be switched, and its capacitance is independent of applied voltage. By using multiple switches, the voltage of the tracked analog signal is captured as charge and isolated. The captured charge is flown (switched to another circuit where that sampled voltage is used) by transmission-gate switches on both ends of the flying

capacitor. Flying capacitors are constructed from on-chip interconnect fringe capacitance using cordwood stacked interconnect. Because of the high-quality insulator between interconnect, their capacitance does not change over the range of the applied voltage. Jitter-free samples, independent of their signal amplitude, are routinely produced down to the logic's capability as illustrated in Figure **3**.

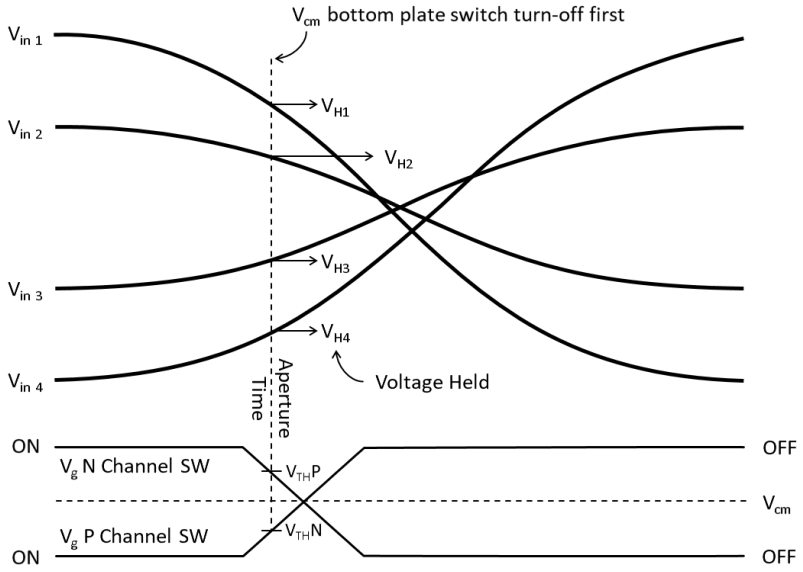

Figure **3.1** – *Bottom-Plate disconnect freezes aperture time independent of analog voltage on top-plate when bottom-plate is operated at ~mid-logic analog V_{cm} ground*

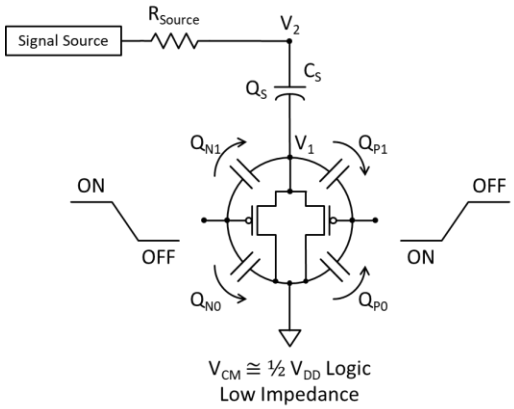

Figure **3.2** – *Transmission-gate switch turnoff charge transfer capacitances*

Relative transmission-gate AC termination impedances determine the charge transfer division;
(Q_{N1} - Q_{P1}) ↔ onto Q_S creates an error on V1 because Qs is DC isolated after switching.
Q_{NO} & Q_{PO} are irrelevant because they transfer their charge into a low impedance.

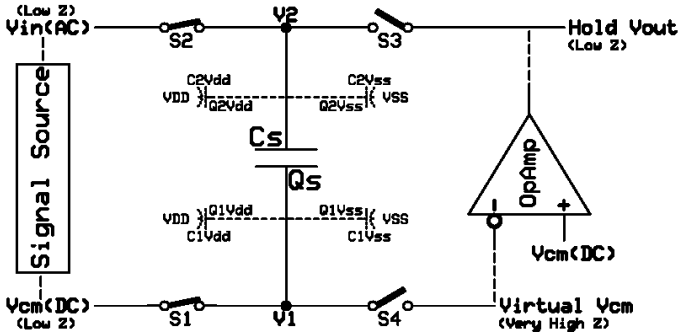

Figure **4** – *Track and Hold – Fundamental Switch Operation with parasitic capacitances /charges*

Sequential switch operation:

1. Switch **S1** opens first at the precise logically defined aperture time to fix the charge **Qs** on **Cs** by initiating a high series impedance on the bottom-plate of tracking capacitor **Cs** thus isolating its charge **Qs**. Note that this initial switch operation is independent of signal voltage because the turn-off threshold of **S1** is referenced to the DC common-mode analog signal ground **Vcm**, which is biased near ½ of the logic supply voltage (Vdd-Vss)/2 so that the complementary advantages of transmission-gate switches can be embodied.

2. Next, switch **S2** opens at a logic buffer delay after **S1** is opened to disconnect **Vin** from the signal source. Any charge transfer to **Cs** slightly moves the **V1** to **V2** voltage across **Cs**, but because of the high series impedance on the bottom-plate referenced **Qs** is preserved with its initial respect to **Vcm** although **Cs** charge shares with **C1Vdd** and **C1Vss** parasitic capacitance. This **Vcm** referenced **Qs** isolated charge will be treated like a precision battery.

3. Switch **S3** is closed at a short logic-buffer delay after **S2** to prevent current spiking between the **VinAC** signal source and the **OpAmp** output. Because of maintaining a high series impedance on the bottom-plate of **Cs**, its sample charge **Qs** is preserved regardless of what happens on the **Cs** top-plate node **V2**. Top-plate parasitic capacitances **C2Vdd** and **C2Vss** may be altered through the low impedance **S2** and/or **S1** switches, but high series impedance at **S1** to the **Cs** bottom-plate preserves the **Qs** charge henceforth.

4. Switch **S4** follows shortly to close the loop around the **OpAmp**. Because the OpAmp input is biased at the same **Vcm** voltage that the bottom-plate was isolated from, **Cs** bottom-plate parasitics **C1Vdd** and **C1Vss** are returned to their sampled voltages, exactly re-establishing the sample voltage aperture values providing the hold output voltage which becomes valid as the **OpAmp** settles. The **OpAmp** offset voltage is the remaining significant error source which will be taken care of with CiFET-Amplifier and its offset correction techniques covered later in this document.

This method isolates and preserves the charge **Qs** on the tracking capacitor **Cs** and thus its hold voltage by maintaining a high impedance on at least one end of **Cs**. Also, when **Cs** bottom-plate is returned to a virtual **Vcm** when the hold voltage is utilized by handling **Cs**/**Qs** as if it is a precision battery.

Maintaining a series high-impedance on **Cs** and returning its bottom-plate to the cutoff **Vcm** voltage cancels out any parasitic bleeding of charge on **Cs** making **Cs** to appear as a battery that stores the sampled voltage. Also, any

leakage current on the bottom-plate tends to balance out at the mid-voltage used for **Vcm**, extending storage time decay significantly as it dominantly decays to where it needs to be: **Vcm**.

The use of a transmission-gate switch for **S1,** which is connected to the bottom plate of **Cs**, causes **S1** to turn off independently from the active analog signal voltage, as the transmission-gate switching threshold voltages are referenced to a mid-logic voltage and not the signal voltage that can be anywhere from a diode below the bottom rail to a diode above the top rail. An additional advantage of using a transmission-gate where the turn-off charge of the P-channel transmission-gate switch roughly cancels the N-channel's opposite going turn-off charge pass-through. Relative sizing, using nominal simulation model parameters, of these two switches match-cancels the pass-through charge transfers to minimize capacitor size requirements for a given accuracy target. In the CiFET CiAmp implementation Figure **6.3** and **6.4**, both **S1a** and **S1c** are these balanced transmission gates. The minimum **Cs** capacitance value is then limited to the theoretical KT/Cs Boltzmann noise floor which is RMS related to the overall analog signal voltage range.

General logic IC process implementation principals in the order of their significance:

1. Capacitors consume lots of IC real estate and settle relatively slow;
2. Switches are small and fast;
3. Transmission-gate switches can be easily balanced when operated with their channel voltage around ½ of their logic supply;
4. Complementary circuitry tends to leak towards ~½ their power supply where they are biased.

The **first** level of Track & Hold error source occurs at the time when the controlling gate logic voltage is a threshold away from the analog voltage in the channel, making the turnoff aperture time a function of the tracked voltage. As shown in Fig. **3** this uncertainty is eliminated by connecting the tracking capacitor bottom-plate to an analog common-mode voltage Vcm located near the mid-voltage of the logic supply voltage.

The **second** level of Track & Hold error source is caused by charge transfer from the switch gate control logic onto the analog channel terminating on the hold capacitor **Cs** in Fig **1.0**. The solution to this problem simply adds a small capacitance to remove this charge error on the tracking capacitor **Cs** by coupling an opposing logic transition onto **Cs**. A dummy switch of half the size with opposing gate control logic has been be used to control access to this trimming capacitor, but the small increase in complexity often adds additional things to go wrong as a Monte-Carlo analysis will reveal. These fixes vary with the tracked analog voltage. By using a complementary MOSFET transmission gate switch to open the analog ground Vcm on the bottom-plate switch enables capacitive symmetry cancellation. There are some other active charge-transfer methods which are often worse than just nominally balancing the transmission-gate switch charge transfers.

The **third** level, and last of the significant error source types of Track & Hold errors are caused by parasitic capacitances on both terminals of the tacking capacitor Cs. These capacitances are indicated by the two ghost capacitors in each of Figure **5** as **C1** and **C2**. In the Circuit Seed Track & Hold, this error is all but eliminated by maintaining a high-impedance on at least one end of the tracking capacitor **Cs** from tracking cutoff time period **T2** and returning the tracking capacitor **Cs** bottom-plate **V1** to analog ground **Vcm** during the time period **T5** when the "Hold-Voltage" is valid for use by the subsequent circuitry such as an ADC in Figure **1**. Since the bottom-plate voltage **V1** is sampled at **Vcm**, and flown back to an equivalent virtual **Vcm** later in **T5**, while maintaining a high series impedance on the bottom plate offered by the OpAmp high-impedance input and open switch **S1**, the parasitic charge-sharing errors of **Q1Vdd** and **Q1Vss** to alter the charge **Q1** on **C1** are nullified, thus zeroing out **Qs** charge sharing errors.

The top-plate parasitic capacitance ends up in parallel with the low impedance amplifier output along with any loading and as long as the other terminal of Cs remains in high impedance, this charge does not modify **Qs**.

In isolating and maintaining a precise sampled charge **Qs**, several considerations are sequentially applied to a track and hold switching sequence. An example logic clocking circuit that enacts this is included in Figure **10**, where a differential S/H technique is shown. In Fig **2.0** the all-important switching sequence is outlined for each of five successive time increments **T1** – **T5**. Each incremental time period must be long enough to provide the necessary number of time constants to settle to the specified precision. The significance of each of these 5 incremental time steps is defined by how their time windows are terminated. The state diagram of these 5 states is diagrammed in **Figure 5** and **Table 1**:

As a walkthrough of the process from the analog signal ***tracking*** **T1** to that sample being presented for ***utilization*** **T5**, consider Figure **4** and **5** together. At a precise logically determined sample aperture time **T2**, which is accurate to logic jitter noise, the tracking capacitor's bottom-plate terminal is disconnected initially by opening **Sw1** before the top-plate terminal is disconnected in **T3** by **Sw2** at a logic buffer delay later. **Sw3** and **Sw4** are open at this time. As such, the tracking capacitor **Cs** traps an instantons aperture-time voltage sampled as charge **Qs.** This charge is isolated in **T2** at the aperture time, when its bottom-plate parasitic capacitances **C1Vdd** & **C1Vss** were charged to **Vcm**. This analog signal input is then disconnected in **T2** to float the tracking capacitor **Cs** so that it can be rearranged to a different connection for **T3** and **T4**.

At **T3**, the disconnected top-plate of **Cs** is flown to the **OpAmp** output by closing switch **S3** while maintaining a high series resistance path to **Cs**. At a logic buffer delay **T4,** the bottom-plate of **Cs** is connected to the high-impedance **OpAmp** input which is actively biased at a virtual V**cm.** This virtual Vcm reconnect restores any charge sharing errors bled off on **C1Vdd** and **C1Vss**, and a high **Cs** series resistance maintains the voltage (Vs=Qs/Cs). Thus, in T5, the buffered analog hold voltage is presented to an external utilization circuit such as an ADC.

Once that voltage is utilized, the switches revert to the position where the analog input voltage is tracked **T1**, and the switching sequence can again occur to produce another hold voltage sample to be presented to the subsequent analog signal processing circuitry a cycle time later. High series impedance is maintained on at least one side of the sample capacitor to isolate its charge, and thus the capacitor with its stored charge becomes a stored voltage.

During tracking, the parasitic capacitance related to the tracking capacitor **Cs** bottom-plate was hard-referenced to **Vcm** by a switch **Sw1**, which is located near ½ of the logic power supply voltage, and then re-referenced to Vcm by the OpAmp inputs biased around the same virtual ground for utilization.

A Track & Hold circuit simply tracks an analog input voltage and freezes its instantaneous value under logic command and buffers the hold voltage for subsequent analog processing circuitry. The delay variability from the logic hold command to freezing the analog voltage defines its jitter, which must be substantially independent of instantaneous signal magnitude or frequency content.

Circuit-Seed Track & Hold implementations achieve this objective by focusing on charge **Qs** stored on the tracking capacitor **Cs**. At sample aperture time, the sampled charge **Qs** on the tracking capacitor **Cs** is isolated from analog ground and preserved throughout the remainder of the Track & Hold period by maintaining high impedance on at least one end of the tracking capacitor **Cs**.

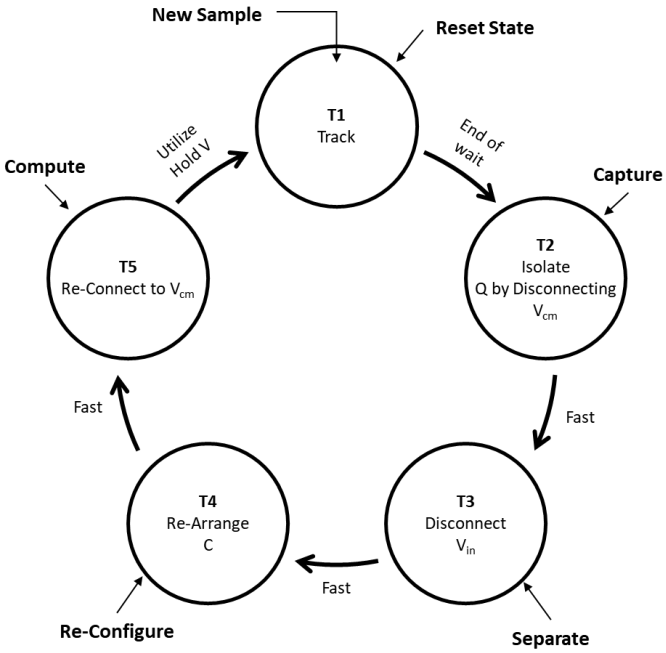

Figure **5** – *Track & Hold state diagram*

This sequence from track to hold, as is broken up into five logically timed event windows summarized in Table **1**:

Time	Switch **1**	Switch **2**	Switch **3**	Switch **4**	Operation
Period	Common Mode	Signal Input	Amp Output	Amp Input	
T1	***Closed***	***Closed***	Open	Open	Track input voltage onto capacitor
T2	Open	***Closed***	Open	Open	Isolate capacitor from analog ground (V_{cm})
T3	Open	Open	Open	Open	Disconnect capacitor from input voltage
T4	Open	Open	***Closed***	Open	Connect input side of capacitor to amplifier output
T5	Open	Open	***Closed***	***Closed***	Connect ground side of capacitor to V_{cm} biased amplifier input

Table **1** – *Track & Hold state summary*

The four switches of Table **1** are identified in Figure **6** as **S1**, **S2**, **S3**, and **S4** in their tracking mode **T1** position along with tracking capacitor **Cs** having a charge **Qs**, a signal source, with a differential OpAmp biased around analog ground **Vcm**. Node **V1** and **V2** parasitic capacitances **Cp1** and **Cp2** charge-share with tracking capacitor **Cs**. Capacitor connections with their charge are stacked in Figure **6.2** and a single-ended CiFET OpAmp implementation example of the track & hold circuit is Figure **6.3**. For a numerical feel, the tracking capacitor may be about 10pf and the parasitic Cp1 and Cp2 have values of about 100fF.

Sequencing through the five **T1** through **T5** track & hold states, operates the individual switches in accordance with Table **1** as illustrated in Figures **6** to **9**. The important time of each **Tn** state is their termination. The duration of the **Tn** period of time is the settling time from entering their state from the previous state.

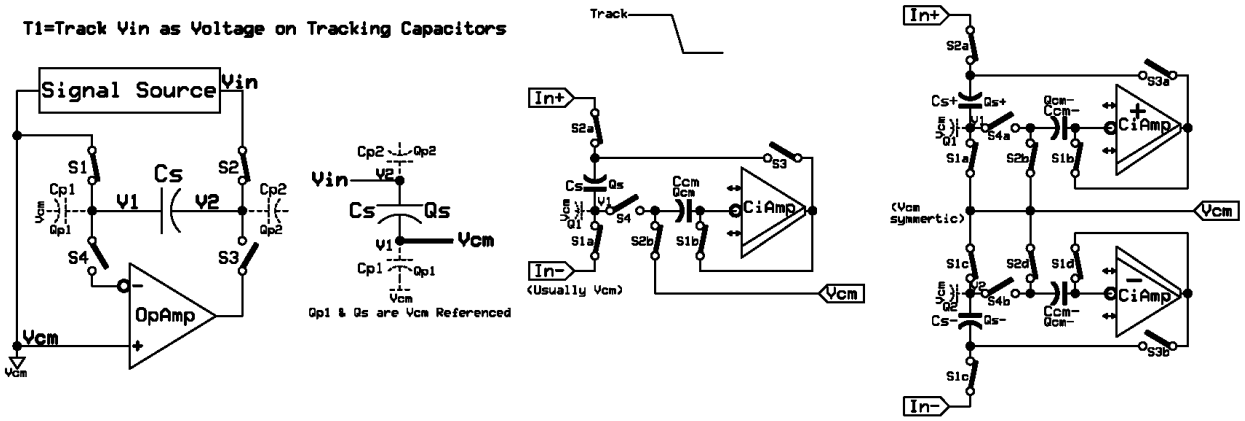

Figure **6.1 - 6.4** – *State **T1** = Track signal source voltage*

Figure **6** represents the tracking state switch positions.
Figure **6.1** is a high-level OpAmp circuit description of the Track & Hold circuit. Figure **6.2** is an operative capacitor simplification that includes the parasitic capacitances **Cp1** and **Cp2.** Figure **6.3** is a mapping of the track & hold circuit onto a single-ended CiFET OpAmp (CiAmp) implementation including additional switches for offset and 1/f noise correction using capacitor **Ccm**. Fig **6.4** is a replica-differential CiFET OpAmp S/H implementation.

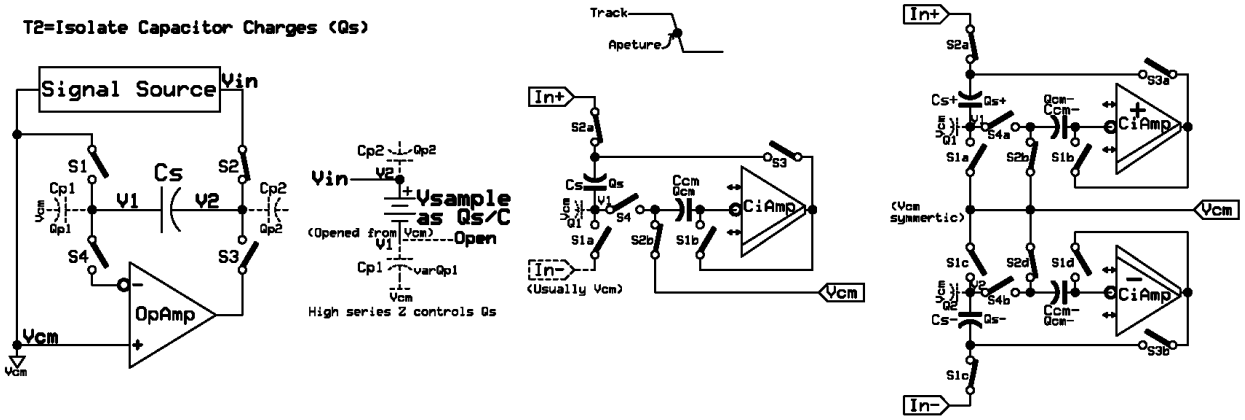

Figure **7.1 – 7.4** – *State **T2** = Isolate tracking capacitor(s) from analog ground (**Vcm**) first*

Figure **7** illustrates the sample aperture cutoff time switch positions.
Figure **7** illustrates track & hold aperture termination of a **T1** tracking period. The analog ground (**Vcm**) is disconnected first at the end of **T1**, making this aperture time independent of the analog voltage which is still connected to the signal source node of the tracking capacitor **Cs**. In all states after **T1**, the sampling capacitor has at least one maintained in a high impedance so that its sampled charge **Qs** is locked on Cs and thus the voltage (**V2**-**V1**) across **Cs** is maintained.

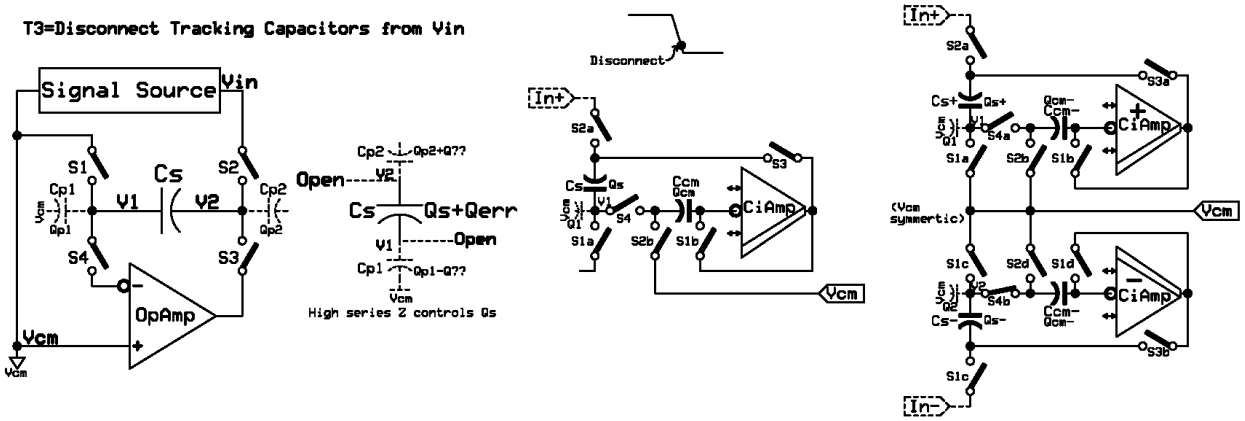

Figure **8.1 - 8.4** – *State **T3** = Disconnect Vin from signal source*

Figure **8** shows the disconnect input switch positions.
Figure **8** illustrates track & hold in its **T3** state in which Cs is disconnected from the signal source. Here the sampling capacitor is completely disconnected and floats or flies-to briefly before its reconnection around the Amplifier as Sw3 is first closed and then **Sw4** is closed finally in state **T5**.

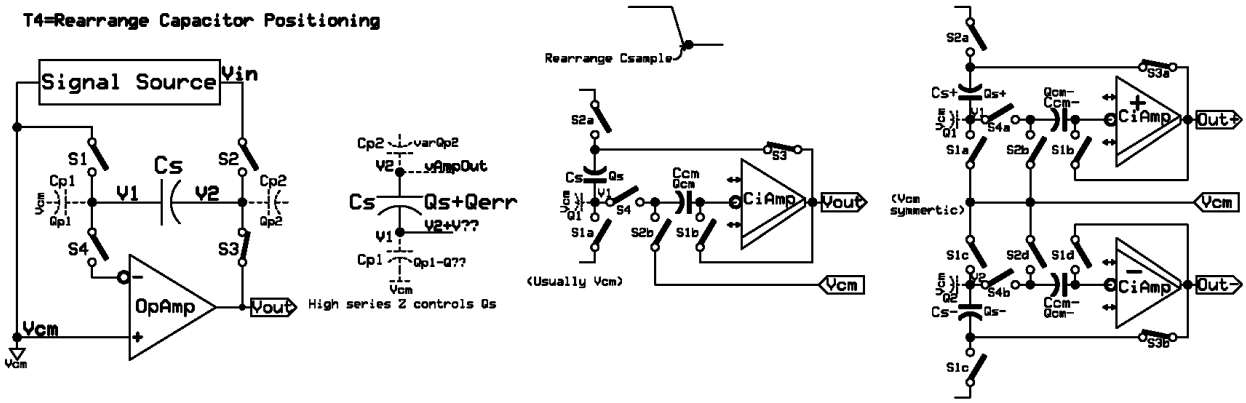

Figure **9.1 - 9.4** – *State **T4** = Rearrange capacitor(s) around amplifier output*

Figure **9** illustrates capacitor connection to OpAmp output, but not yet the capacitor input connected.
Figure **9** above illustrates track & hold in its **T4** state where the sampling capacitor top plate is connected to the amplifier output which is low impedance. Here, the bottom plate is at high impedance as this high impedance holds the sampled **Qs** and any small charge error from **Q2** on the bottom plate parasitic capacitance.

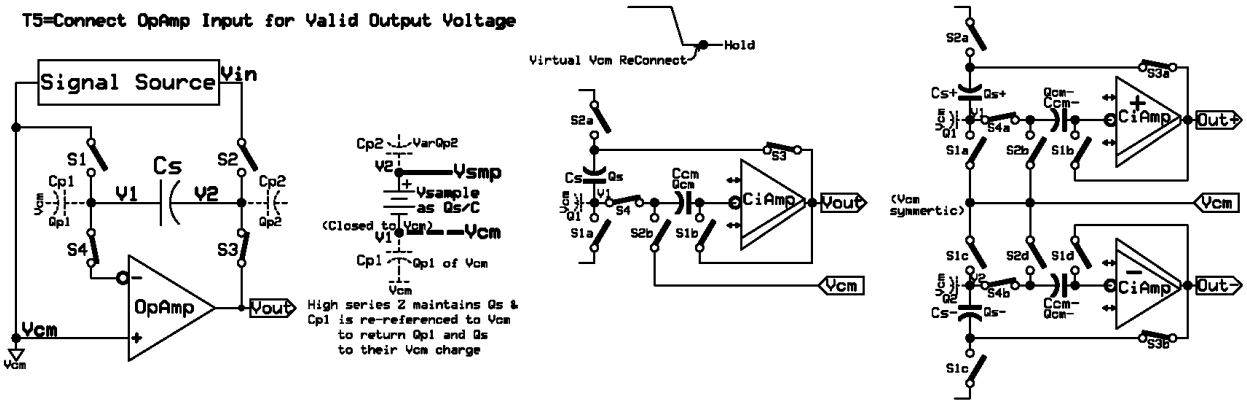

Figure **10.1 - 10.4** – *State **T5** = Sw4 closes and finishes the flying capacitors reconnection to **Vcm** biased amplifier input.*

Figure **10** above illustrates track & hold in its **T5** state which re-established the bottom plate to Vcm, thus removing **Q2** charge shared error on **Cs**. The amplifier input maintains high impedance which has maintained **Qs** charge eliminating sampled voltage errors. A capacitively symmetric transmission gate switch with its complementary gate drives of Figure **11** below is used for the final reconnect switch **S4**.

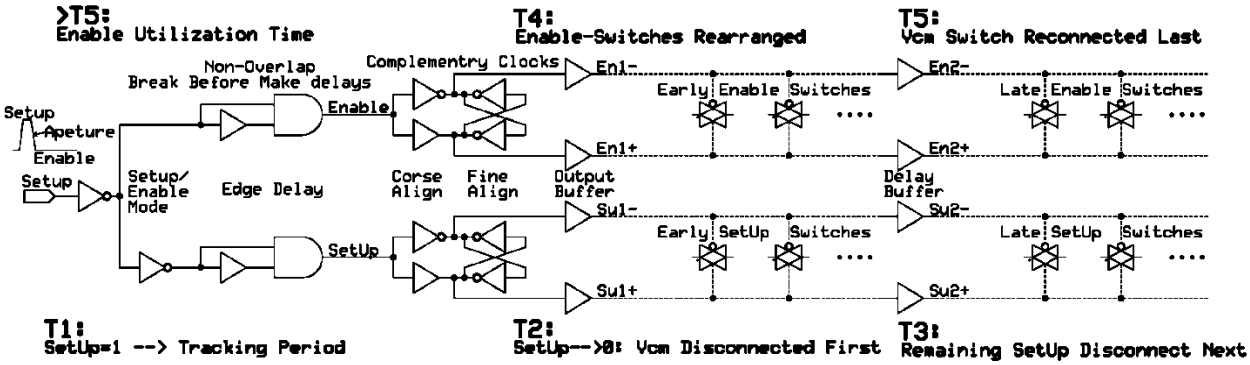

Figure **11** – *Transmission-Gate switch control logic shaping and alignment buffer*

A single logic input "Setup" controls the entire switch sequence. High logic input maintains the Track & Hold circuit in an input voltage tracking mode of operation **T1** where the analog input voltage is applied across the tracking capacitor **Cs** which occurs at essentially at the midpoint of the Setup logic's falling edge. This is where the switching circuit has its most precise resolution in time. Here, the bottom-plate of the tracking capacitor **Cs** is disconnected from **Vcm** using a capacitively symmetric (~equal capacitive coupling from the control logic gates to the analog conducting channel) transmission gate switch. The lower path of the clock driver logic circuit performs this timing to **Su1+** and **Su1-** providing a midpoint complementary gate drive pair of signals to the early setup disconnection switch **S1** to end the tracking time period at the end of **T1**. The charge **Qs** is established by this early step and **Qs** is maintained throughout the rest of the hold time by maintaining a high series resistance with at least one end of **Cs** at all times. There is some temporary charge sharing of **Qs** with its surrounding parasitic capacitances, but **Qs** charge shared errors are brought back to their initial **Vcm** starting point cutoff voltage when the valid hold output is established in **T5**. A logic buffer delay later, **Su2+** and **Su**2- gate logic control signals symmetrically disconnect the top plate of the sampling capacitor **Cs** to isolate it from the analog input signal source. Any change in top plate voltage pulls the bottom plate along with it as the sampling capacitor is acting like a battery throughout the rest of the tack & hold cycle.

For information in regards to licensing, please contact:

Keith Taylor
Vice President Acquisition & Licensing
ktaylor@inventionshare.com
(613) 225-7236 Ext. 105