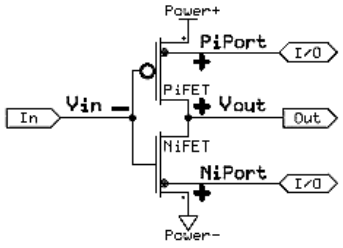
Circuit Seed™

Planting the Future of Electronic Designs

Complementary Current Field Effect Transistor (CiFET™)

Part of the Circuit Seed™ Family of Inventions

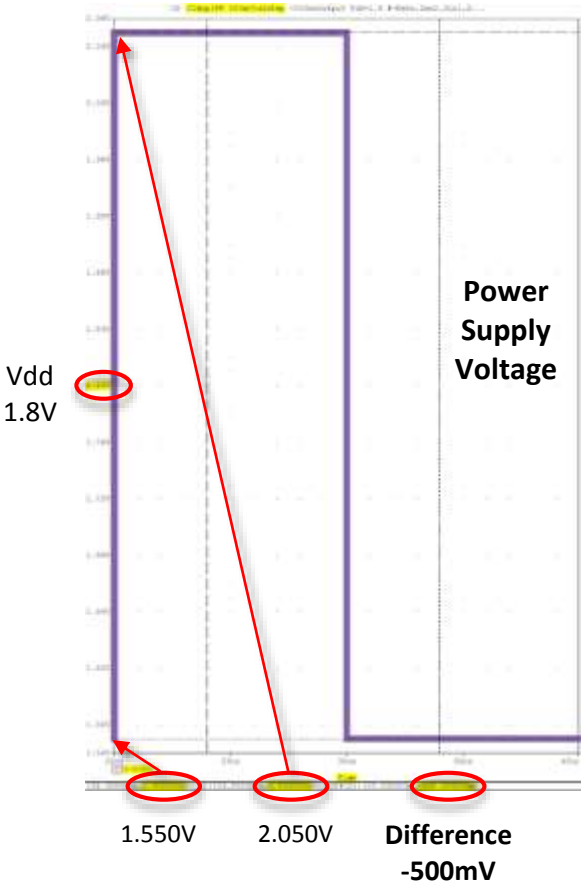
Complementary Current Field Effect Transistor

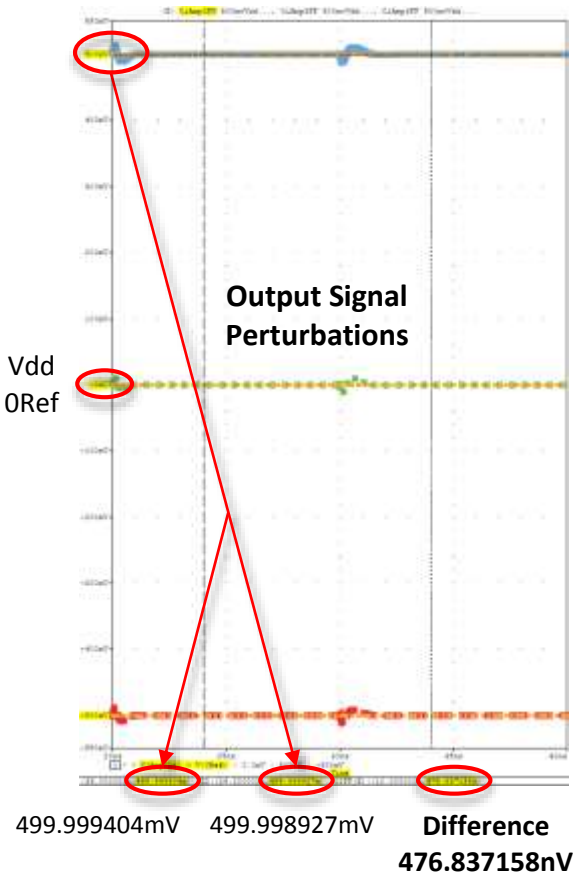


The CiFET™ gets used in a new and revolutionary way, different than that of conventional analog CMOS. It possesses a wide range of potential applications due to its highly desirable characteristics such as flexibility, low power operation, high gain, linearity, low noise, compact area, and increased speed.

When used properly, this novel structure is immune to the power supply noise getting into the signal path. The CiFET™ charge mode analog concept does not reference the power supplies which have the switching noise of digital logic riding on them. Here the example 3 stage feed-forward amplifier using the circuit (CiAmp™) is used to illustrate properties of the Circuit Seed™ analog designs.

500mV Vdd Step and CiAmp™ output perturbation at +500mV, 0.0mV, and -500mV signals





These waveforms illustrate an over-the-top amount of power disturbance. To go beyond any possible level of doubt, a 500mV 0.1ps Rise time step in power supply voltage was imposed – which created about 1 PPM (part-per-million) error in the output signal.
As far as we know this is rather unheard of. Traditional analog CMOS would completely stop working with this much power supply deviation.

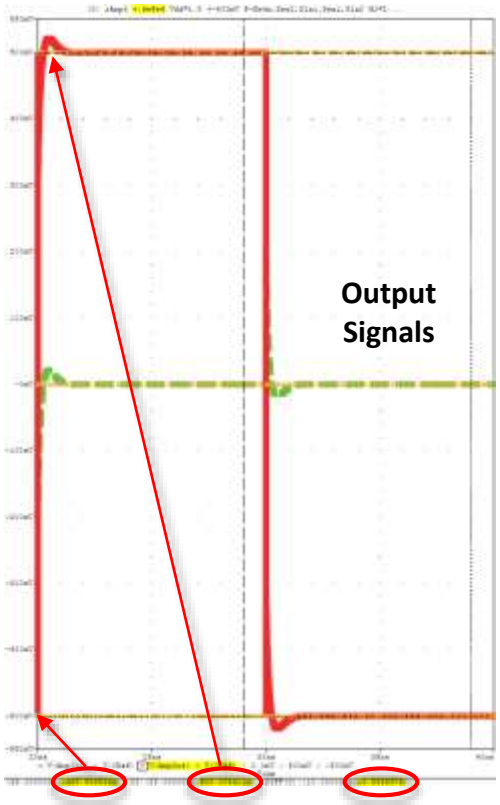
CiAmp™ worst-case IC process parameter corners

These are the worst-case process corners (variation of fabrication parameters). The changes imposed by process corner deviation is almost undetectable in terms of PPM.

Variable / Stage	Channel	+Target Error [PPM]	-Target Error [PPM]	Total Amplitude	Deviation [PPM]	Modify Notes:
1 = Typical	All	-0.83	-0.72	-0.999000002	IC Process	Nominal Baseline
2 = Slow - Slow	All	-2.50	-1.79	-0.999000004	IC Process	Deviation due to Worst Case **4-Corner** IC Process Parameter Limits
3 = Fast - Fast	All	-0.33	-0.24	-0.999000001	IC Process	
4 = Fast N - Slow P	All	1.61	-0.83	-0.999000002	IC Process	
5 = Slow N - Fast P	All	-0.60	-0.89	-0.999000002	IC Process	

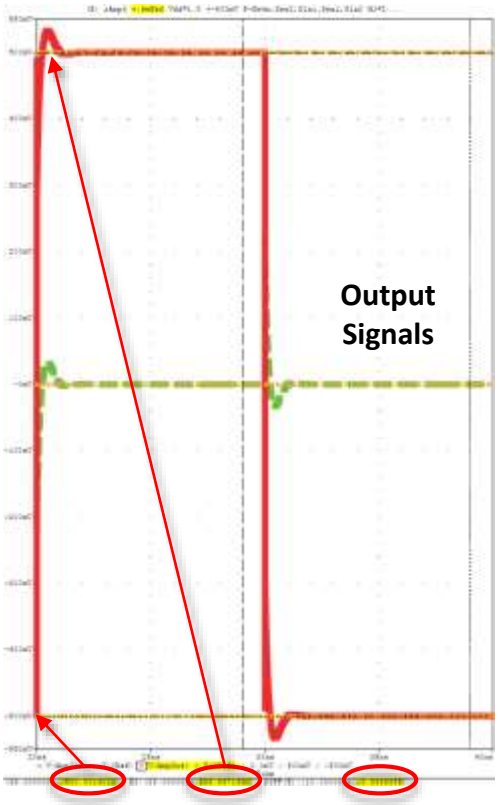
CiAmp ±1.0 volt pulsed response waveform examples for individual 1.5x channel widening

+50%w P Channel-Source Feed Forward



-499.993533mV 500.004411mV **Difference -0.9999979**

+50%w N Channel-Source Output



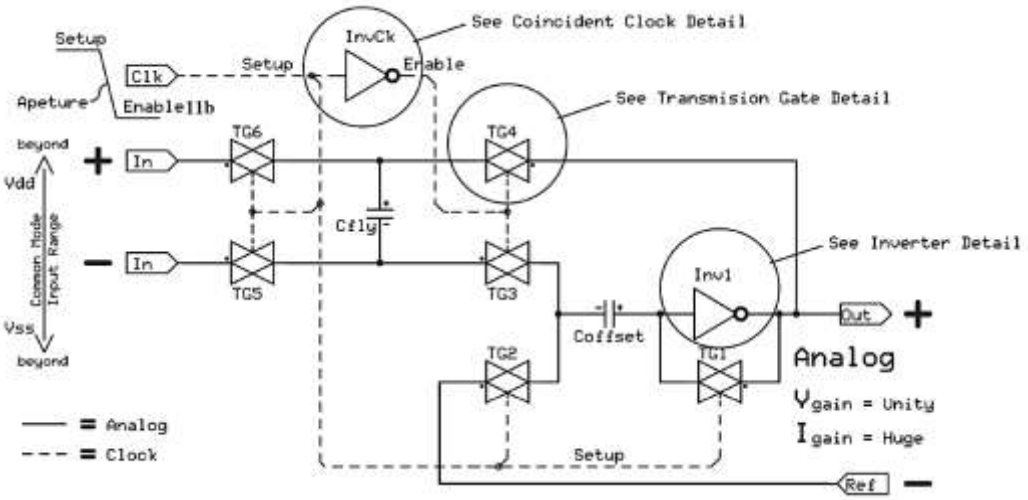
-500.001401mV 499.997139mV **Difference -0.9999985**

One of the major issues that the industry is currently working on is: when integrating single chip systems, the parametric differences and drifts of individual transistors tends to cause significant problems with conventional analog designs. Circuit Seed™ has overcome this problem with an elegant and simple configuration. In order to demonstrate this solution, to an over-kill level, each of the CiFET™ amplifier's channels was increased by **50%** individually.

Variable / Stage	Channel	+Target Error [PPM]	-Target Error [PPM]	Total Amplitude	Deviation [PPM] [50%]	Modify Notes:
Feed Forward	N-Source 4	4.14	-6.32	-0.999000002	1.5*Ns4	Deviation due to individual **channel width** increased by **50%** (one at a time).
Feed Forward	N-Drain 4	-0.24	-1.07	-0.999000001	1.5*Nd4	
Feed Forward	P-Drain 4	-1.46	0.12	-0.999000001	1.5*Pd4	
Feed Forward	P-Source 4	-6.47	4.41	-0.999000002	1.5*Ps4	
3=Output	N-Source 3	1.40	-2.86	-0.999000002	1.5*Ns4	
3=Output	N-Drain 3	-0.51	-0.83	-0.999000001	1.5*Nd4	
3=Output	P-Drain 3	-1.13	-0.24	-0.999000001	1.5*Pd4	
3=Output	P-Source 3	-3.01	1.67	-0.999000001	1.5*Ps4	
2=Slow Dominant	N-Source 2	-295.76	293.85	-0.999000002	1.5*Ns4	
2=Slow Dominant	N-Drain 2	-31.95	30.76	-0.999000001	1.5*Nd4	
2=Slow Dominant	P-Drain 2	42.89	-44.23	-0.999000001	1.5*Pd4	
2=Slow Dominant	P-Source 2	293.61	-295.28	-0.999000002	1.5*Ps4	
1=Input	N-Source 1	38,650.25	-38,652.42 -3.86%	-0.999000002	1.5*Ns1	
1=Input	N-Drain 1	4,124.19	-4,125.48 -0.41%	-0.999000001	1.5*Nd1	
1=Input	P-Drain 1	-5,762.85	5,761.62 0.57%	-0.999000001	1.5*Pd1	
1=Input	P-Source 1	-39,142.25	39,140.11 3.91%	-0.999000002	1.5*Ps1	

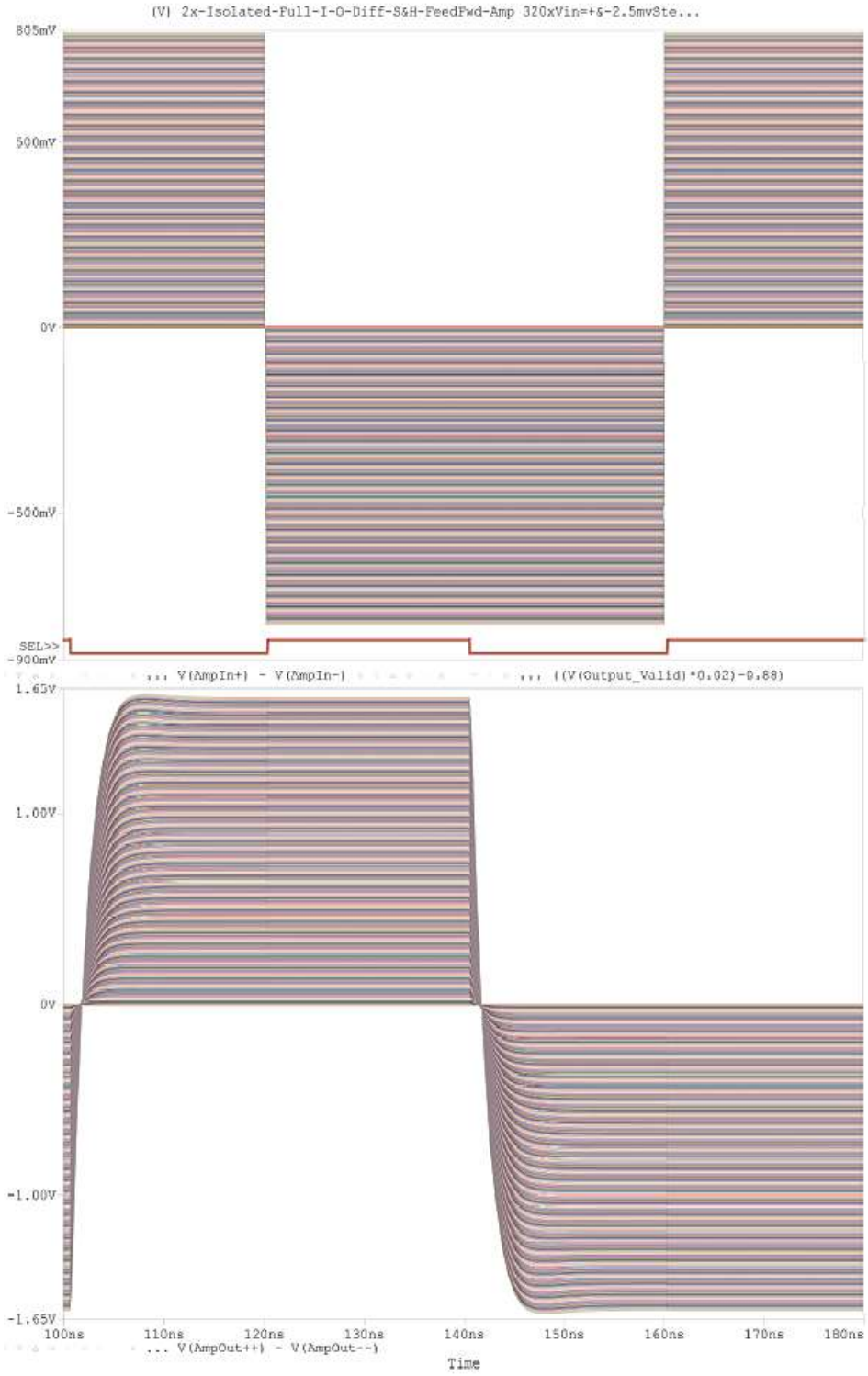
Note that the input stage collects nearly all of the amplifier's deviation. Note that the total amplifier output deviation is on the order of **one PPM** for all of the extreme conditions tried as referenced to the nominal case. This is taken care of by correlated double sampling for the broad ADC class of CiAmp™ usage as indicated in the patent US 9,160,293. (This squelches poor transistor threshold matching which is documented to deviate more than 45mv over life.)

Basic Abstract Amplifier Diagram

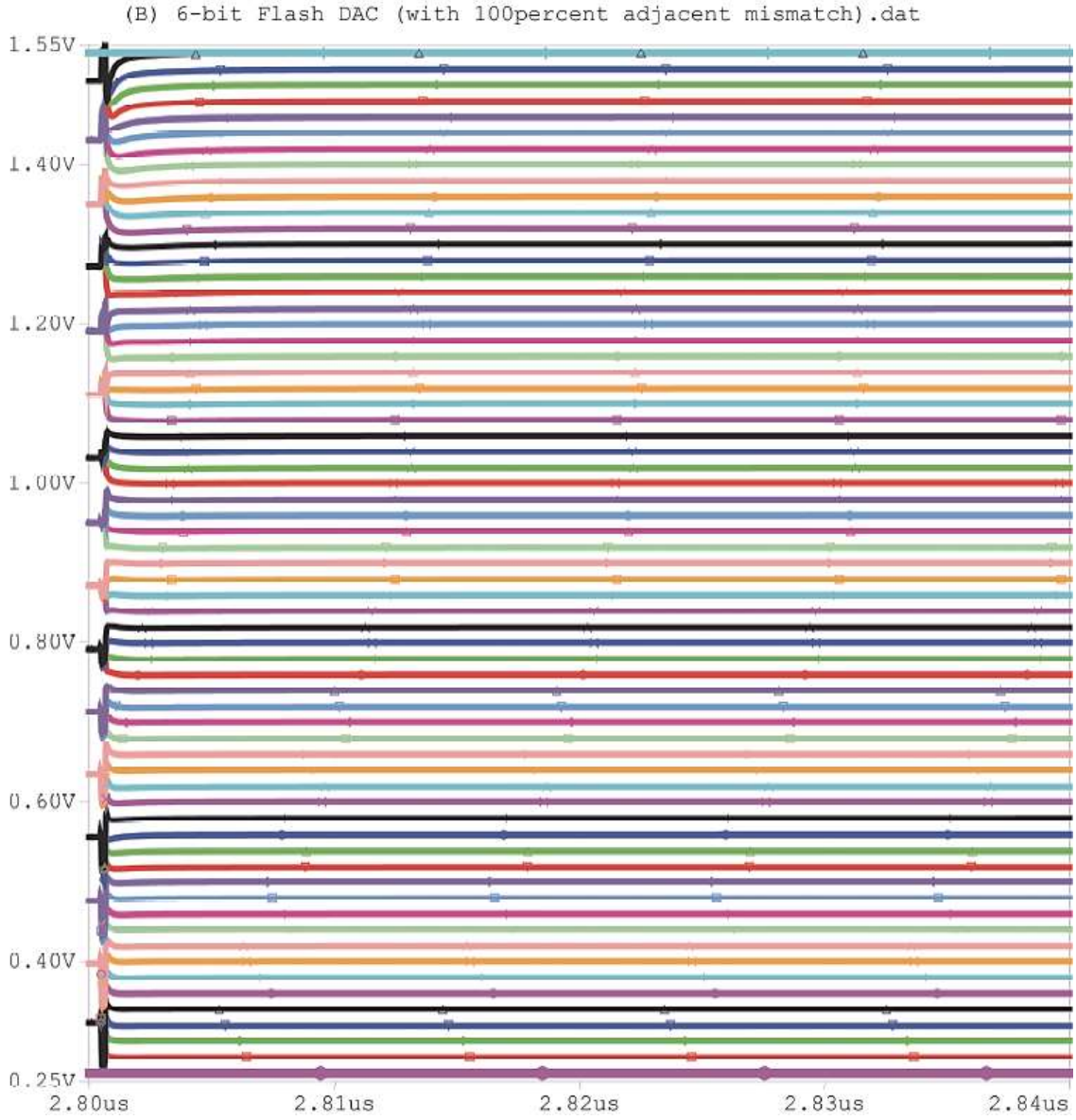


2X Differential Test Chip Schematic Waveform

This is a high precision amplifier (sample & hold) with a stable response at 50 Mega samples per second (320 +/-2.5mV steps@700mV common mode).



This is an example of 100% difference in adjacent component matching tolerance somewhere around the 2/3 level point. The error is undetectable to better than a PPM. No precision parts or trimmed components are required, facilitating precise divisions of the input voltage reference (64 steps of 20mV) as well as enabling other very precise analog operations without precision parts.



The CiFET™ is a Charge-Mode Logic (CCML) device:

The CiFET™ amplifier will probably be the most important and widely used analog building block needed for analog inclusion on digital chips which perform most of the analog signal processing in the digital domain. Impressive operations are available in the digital domain that are not realizable in the analog domain, but higher speed operations can only be implemented in the analog domain. However, there is always a conversion needed between the analog and digital domain for predominantly digital systems.

Most of the time, there is the need for a quality ADC (Analog-to-Digital Converter) and DAC (Digital-to-Analog Converter) to convert between the real world and the digital processor. It makes sense to convert the analog signals into the digital domain as early as possible, thus the sampled data approach. Also, correlated double sampling of the amplifiers and comparators patent eliminate the 1/frequency noise which is most prevalent in MOS transistors. The combination and configuration of these circuits with the ability for the CiFET™ to perform on smaller ICs is the focus of Circuit Seed™.

The CiFET™ in itself exhibits various distinctions including noise considerations all of which are virtually eliminated by the amplifier circuit. No precision parts are required in the CiFET™ amplifier circuits. The circuit is made entirely from digital parts and occupies a small footprint consistent with digital logic rather than analog circuitry. The amplifier is just one example of Circuit Seed™ proprietary sample data circuits which serve various continuous time, and sampled data functions.

Circuit Seed™ also has methods of trading off speed vs. power electrically. A standby state is also available. Analog can be put to sleep and turned back on at logic speeds to immediately operate at its high precision level, unlike any analog circuit.

Because this CCML logic is CiFET™ based, it can be operated with power supplies down to well below 100 millivolts with substantial performance and simulation results demonstrate its operation at 1mV, using 1KHz clock.