FEATURES AS TESTED

CiOpAmp Supply Voltage: 500mV to 1.2V
CiTIA Supply voltage: 10mV to 1.2V
Operating temperature: -55°C to +125°C
Input current: ~10pA to ~10µA
Low power: ~3µA @ 1 Volt V_DD (3µW)
Auto-Zero Clock: 1µs pulse width @1 second period (CiOpAmp)
Offset voltage: ~20nV (CiOpAmp)
Bandwidth: ~200KHz with 60pf and 50kΩ load

TYPICAL APPLICATIONS

CiTIA
Telecommunications
Low Noise Preamplifiers (LNA)
Combined Analog and Digital System-on-Chip (SoC)
Signal Isolator
Sensing
Modulation/Demodulation
Logic Signal Transmission
Bus Line Receiver
Accurate and fast Analog Signal Level Transmission
Fiber Optic Receiver
and more

CiOpAmp
Single-ended Operational Amplifiers (OpAmps)
Differential Low Noise Amplifier (LNA)
Proportional to Temperature Reference (PTAT)
Phase-Locked-Loop (PLL)
Ring Oscillator with Ultra-High Spectral Purity
Multi-GHz Ring Voltage Controlled Oscillator (VCO)
Frequency Mixers
Combined Analog and Digital System-on-Chip (SoC)
Internet of Things (IoT)
Memory and Processors
Voltage/Temperature Referencing
Analog-to-Digital Conversion (ADC)
Digital-to-Analog Conversion (DAC)
Sensing
Modulation/Demodulation
and more

DESCRIPTION

This document is to help serve as an explanation for the basic testing of the Enigma IC. Also, contained in this document are snapshot of the schematics and layout for testing of the 4 basic circuits of interest on the Enigma IC:

Block 1—CiTIA (100Ω input impedance)
Block 2—CiTIA (4kΩ input impedance)
Block 3—CiOpAmp (0.2pf capacitors)
Block 4—CiOpAmp (10pf capacitors)

The first 2 circuits are CiFET-based differential transimpedance amplifiers, one with the CiFETs (i.e. Complementary injection Field Effect Transistors) sized for an 100Ω input impedance and the latter sized for a 4kΩ input impedance, both at the complementary iPorts. The last 2 circuits are CiFET-based differential OpAmps, the first with a smaller 0.2pf capacitors, and the last, with larger 10pF capacitors.
**SPECIFICATIONS**

\( T_A = 25^\circ C, \) Enigma IC, GF 130nm CMOS Technology, Test Results

<table>
<thead>
<tr>
<th>Description</th>
<th>Mnemonic</th>
<th>CiOpAmp</th>
<th>CiTIA</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply Voltage (+)</td>
<td>( V_{DD} )</td>
<td>0.5</td>
<td>1.2</td>
<td>0.01</td>
</tr>
<tr>
<td>Supply Voltage (-)</td>
<td>( V_{SS} )</td>
<td>GND</td>
<td>GND</td>
<td>GND</td>
</tr>
<tr>
<td>Supply Current</td>
<td></td>
<td>3-pico</td>
<td>20µA</td>
<td>3-pico</td>
</tr>
<tr>
<td>Input Voltage Range</td>
<td>( V_{in} )</td>
<td>0</td>
<td>±1.5</td>
<td>0</td>
</tr>
<tr>
<td>Input Offset Voltage</td>
<td>( V_{OS} )</td>
<td>±0.02</td>
<td>±3.5</td>
<td>-</td>
</tr>
<tr>
<td>Input Current</td>
<td>( I_{in} )</td>
<td>High Z</td>
<td>High Z</td>
<td>0</td>
</tr>
<tr>
<td>Input Resistance</td>
<td>( R_{in} )</td>
<td>&gt;10MΩ</td>
<td>100GΩ</td>
<td>&gt;25Ω</td>
</tr>
<tr>
<td>Output Voltage Swing</td>
<td>( V_{OUT} )</td>
<td>( V_{DD} ) - 200m</td>
<td>( V_{DD} ) - 10m</td>
<td>( V_{DD} ) - 5m</td>
</tr>
<tr>
<td>Output Current</td>
<td>( I_{OUT} )</td>
<td>5µA</td>
<td>10µA</td>
<td>5µA</td>
</tr>
<tr>
<td>Power Consumption</td>
<td>( P_Q )</td>
<td>1-pico</td>
<td>20µA</td>
<td>1µA</td>
</tr>
<tr>
<td>Transient Response</td>
<td>Rise Time</td>
<td>( T_r )</td>
<td>-</td>
<td>200</td>
</tr>
<tr>
<td></td>
<td>Overshoot</td>
<td>( M_P )</td>
<td>0</td>
<td>5</td>
</tr>
<tr>
<td>Frequency Range*</td>
<td>( f )</td>
<td>0</td>
<td>200</td>
<td>0</td>
</tr>
<tr>
<td>Close-Loop Gain</td>
<td>( A_{in}, A_v )</td>
<td>20dB</td>
<td>20dB</td>
<td>80mV/µA</td>
</tr>
</tbody>
</table>

*Frequency range is limited by the test pads, simulation results illustrate a multi-GHz operation for the CiTIA and hundreds of MHz for the CiOpAmp at 130nm. Simulations appear to stretch this out into GHz region at smaller process nodes. Speed is proportional to ring oscillator speed.
Performance Characteristics

**CiOpAmp 100KΩ, 30pF Load**

$T_A = 25°C$, $V_{DD} = 1.2V$ (unless otherwise noted), clock = $1Hz$ @$1\mu s$ pulse, $V_{in} = 50mV_{rms}$

![Graph showing frequency response at various $V_{DD}$](image-url)

The offset is at its highest due to gain BW at $1V$, where the accuracy of the simulator loses convergence. RelTol needs to be $\sim$100 billion : 1.
Performance Characteristics

CiOpAmp 100KΩ, 30pF Load

$T_A = 25^\circ C$, $V_{DD} = 1.2V$ (unless otherwise noted), clock = 1Hz @1µs pulse, $V_{in} = 50mV_{rms}$
Performance Characteristics

CiOpAmp 100KΩ, 30pF Load

\(T_A = 25°C, V_{DD} = 1.2V\) (unless otherwise noted), clock = 1Hz @1µs pulse, \(V_{in} = 50mV_{rms}\)
Performance Characteristics

CiOpAmp 100KΩ, 30pF Load

$T_A = 25°C$, $V_{DD} = 1.2V$ (unless otherwise noted), clock = 1Hz @1µs pulse, $V_{in} = 50$mV$_{rms}$

Total Harmonic Distortion plus Noise (THD+N) (Test Results)
PERFORMANCE CHARACTERISTICS

CiTIA 100Ω Input Impedance

Audio Precision Equipment, \( T_A = 25°C, \) \( V_{DD} = 1.2V, \) \( R_{in} = 100Ω, \) Load = 60pf and 50kΩ load

+PiPort Input Current vs Output Voltage (Test Results)

+PiPort Input Current vs Input Resistance (Test Results)
PERFORMANCE CHARACTERISTICS

CiTIA 100Ω Input Impedance
Audio Precision Equipment, $T_a = 25^\circ C$, $V_{DD} = 1.2V$, $R_{in} = 100\Omega$, Load = 60pf and 50kΩ load
PERFORMANCE CHARACTERISTICS

CiTIA 100Ω Input Impedance
Audio Precision Equipment, $T_a = 25^\circ C$, $V_{DD} = 1.2V$, $R_{in} = 100\Omega$, Load = 60pf and 50kΩ load

![PiPort Input Current vs Output Voltage (Test Results)](image1.png)

![PiPort Input Current vs Input Resistance (Test Results)](image2.png)
PERFORMANCE CHARACTERISTICS

CiTIA 100Ω Input Impedance

Audio Precision Equipment, $T_a = 25°C$, $V_{DD} = 1.2V$, $R_{in} = 100Ω$, Load = 60pf and 50kΩ load

-NiPort Input Current vs Output Voltage (Test Results)

-NiPort Input Current vs Input Resistance (Test Results)
CIRCUITS OVERVIEW

CiTIA

These CiTIA circuits are fully integrated into any IC process, including processes without any analog IC process extensions, enabling migration into nanoscale processes nodes. Full levels of integration not only have cost savings, but incorporate a system enhancement advantage provided by on chip processing and communication including RF.

The CiTIA application performs as a general-purpose sensor interface to extract a minute redistribution of electronic charge or the subsequent impedance change within a signal source to be measured electronically.

CiOpAmp

This full-differential CIFET OpAmp is to be a baseline configuration (single-ended or differential single-stage, 2-stage, 3-stage, and 3-stage feed-forward CiAmp can be constructed). Each of the CiAmp arrangements do not use traditional analog current mirrors or state-of-the-art bulky analog transistors for gain, but instead have a low output impedance which drives stiff Resistive and Capacitive loads, is small, low power, and scalable into nanotechnology IC process nodes.
TEST BENCH EXPLANATION

The test bench used to test the CiFETS is shown in the schematic below.

**Known values on the schematic are:**

- Thevenin input voltages \([V_{t}]\)
- Thevenin input resistances \([R_{t}]\)
- Coupling capacitors \([C_{c}]\)
- Load capacitors \([C_{L}]\)

**Unknown values are:**

- Input current \([I_{in}]\)
- Bond pad capacitance \([CBP] \sim 1.7\text{pf}\)
- Input capacitance \([C_{in}]\)
- Input resistance \([R_{in}] \sim 100\Omega \text{ or } 4k\Omega\)
- Output resistance \([R_{out}]\)
- Output capacitance \([C_{out}]\)
- Transimpedance \([Z_{A}]\)

Measured nodes that will produce data are input voltages \([V_{in}]\) and output voltages \([V_{out}]\). Measurements will be made on the oscilloscope in the time domain. Measurements that require divisions in the time domain (which can cause infinite values when the sinusoidal divisor periodically crosses the time axis with a value of “zero” will use amplitude or RMS measurements.
CiOpAmp TYPICAL CONFIGURATION

CiOpAmp CLOCK GENERATOR PERTINENT SCHEMATIC

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TEST BOARD LAYOUT

Wire-bonded, packaged, and fibbed IC pins for the Enigma IC. These should be used for physical testing of the 4 circuits of interest for Circuit Seed.
## PIN CONFIGURATION AND FUNCTIONS

<table>
<thead>
<tr>
<th>Pin#</th>
<th>IC PAD Name</th>
<th>Blocks</th>
</tr>
</thead>
<tbody>
<tr>
<td>94</td>
<td>Analog Ground AVSS (Shared)</td>
<td></td>
</tr>
<tr>
<td>93</td>
<td>X</td>
<td></td>
</tr>
<tr>
<td>92</td>
<td>Analog Drain Supply Voltage AVDD (Shared)</td>
<td></td>
</tr>
<tr>
<td>91</td>
<td>CITIA_100_Vout_Plus</td>
<td>Block 1</td>
</tr>
<tr>
<td>90</td>
<td>CITIA_100_NiPort_Plus</td>
<td>CITIA (100Ω input impedance)</td>
</tr>
<tr>
<td>89</td>
<td>CITIA_100_PiPort_Plus</td>
<td></td>
</tr>
<tr>
<td>88</td>
<td>CITIA_100_PiPort_Minus</td>
<td></td>
</tr>
<tr>
<td>87</td>
<td>CITIA_100_NiPort_Minus</td>
<td></td>
</tr>
<tr>
<td>86</td>
<td>CITIA_100_Vout_Minus</td>
<td></td>
</tr>
<tr>
<td>85</td>
<td>CITIA_4k_Vout_Plus</td>
<td>Block 2</td>
</tr>
<tr>
<td>84</td>
<td>CITIA_4k_NiPort_Plus</td>
<td>CITIA (4kΩ input impedance)</td>
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<tr>
<td>83</td>
<td>CITIA_4k_PiPort_Plus</td>
<td></td>
</tr>
<tr>
<td>82</td>
<td>CITIA_4k_PiPort_Minus</td>
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<td>81</td>
<td>CITIA_4k_NiPort_Minus</td>
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<td>80</td>
<td>CITIA_4k_Vout_Minus</td>
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<tr>
<td>79</td>
<td>X</td>
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</tr>
<tr>
<td>78</td>
<td>X</td>
<td></td>
</tr>
<tr>
<td>77</td>
<td>X</td>
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<tr>
<td>76</td>
<td>CITIA_4k_VZeroRef</td>
<td>Block 2 Cont.</td>
</tr>
<tr>
<td>75</td>
<td>CiOpAmp_2_Vin_Minus</td>
<td>Block 3</td>
</tr>
<tr>
<td>74</td>
<td>CiOpAmp_2_Vin_Plus</td>
<td>CiOpAmp (02pF capacitors)</td>
</tr>
<tr>
<td>73</td>
<td>CiOpAmp_10_Vout_Final_Plus</td>
<td>Block 4</td>
</tr>
<tr>
<td>72</td>
<td>CiOpAmp_10_Vout_Feedback_Plus</td>
<td>CiOpAmp (10pF capacitors)</td>
</tr>
<tr>
<td>71</td>
<td>CiOpAmp_10_Vin_Minus</td>
<td></td>
</tr>
<tr>
<td>70</td>
<td>CiOpAmp_VCM_bias (Shared)</td>
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</tr>
<tr>
<td>69</td>
<td>CiOpAmp_10_Vin_Plus</td>
<td>Block 4 Cont.</td>
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<tr>
<td>68</td>
<td>CiOpAmp_2_Vout_Feedback_Plus</td>
<td>Block 3 Cont.</td>
</tr>
<tr>
<td>67</td>
<td>CiOpAmp_2_Vout_Final_Plus</td>
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<tr>
<td>66</td>
<td>CiOpAmp_2_Vout_Final_Minus</td>
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<td>65</td>
<td>CiOpAmp_2_Vout_Feedback_Minus</td>
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<td>64</td>
<td>CITIA_100_VZeroRef</td>
<td>Block 1 Cont.</td>
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<tr>
<td>63</td>
<td>CiOpAmp_10_Vout_Feedback_Minus</td>
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</tr>
<tr>
<td>62</td>
<td>CiOpAmp_10_Vout_Final_Minus</td>
<td>Block 4 Cont.</td>
</tr>
<tr>
<td>61</td>
<td>CiOpAmp_VCLK (Shared)</td>
<td></td>
</tr>
</tbody>
</table>
FUNCTIONAL BLOCK DIAGRAMS AND PIN CONFIGURATION

Block 1
CiTIA (100Ω input impedance)

Block 2
CiTIA (4kΩ input impedance)

Block 3
CiOpAmp (200ff capacitors)

Block 4
CiOpAmp (10pf Capacitors)
REQUIRED EQUATIONS FOR MAKING MEASUREMENTS

The following equations are used with measurements taken to determine the following low frequency schematic values:

### Input Current

\[
I_{inP+} = \frac{(V_{iP+} - V_{iP-})}{R_t}
\]
\[
I_{inP-} = \frac{(V_{iP-} - V_{iP-})}{R_t}
\]
\[
I_{inN+} = \frac{(V_{iN+} - V_{iN+})}{R_t}
\]
\[
I_{inN-} = \frac{(V_{iN-} - V_{iN-})}{R_t}
\]

### Input Resistance

\[
R_{inP+} = R_t \frac{V_{iP+}}{1 - \frac{V_{iP+}}{V_{iP+}}}
\]
\[
R_{inP-} = R_t \frac{V_{iP-}}{1 - \frac{V_{iP-}}{V_{iP-}}}
\]
\[
R_{inN+} = R_t \frac{V_{iN+}}{1 - \frac{V_{iN+}}{V_{iN+}}}
\]
\[
R_{inN-} = R_t \frac{V_{iN-}}{1 - \frac{V_{iN-}}{V_{iN-}}}
\]

### Transimpedance

\[
Z_{AP+} = R_t \frac{V_{out+}}{V_{iP+} - V_{iP-}}
\]
\[
Z_{AP-} = R_t \frac{V_{out-}}{V_{iP+} - V_{iP-}}
\]
\[
Z_{AN+} = R_t \frac{V_{out+}}{V_{iN+} - V_{iN-}}
\]
\[
Z_{AN-} = R_t \frac{V_{out-}}{V_{iN+} - V_{iN-}}
\]

Adding a load resistance can allow the measurement of the output resistance. It requires determining the transimpedance from Eq. (3) and using the results:

### Output Resistance

\[
R_{out+} = R_L \frac{1 - \frac{V_{out+}}{Z_{AP+}(V_{iP+} - V_{iP-})}}{Z_{AP+}(V_{iP+} - V_{iP-})}
\]
\[
R_{out-} = R_L \frac{1 - \frac{V_{out-}}{Z_{AP-}(V_{iP+} - V_{iP-})}}{Z_{AP-}(V_{iP+} - V_{iP-})}
\]
\[
R_{out+} = R_L \frac{1 - \frac{V_{out+}}{Z_{AN+}(V_{iN+} - V_{iN-})}}{Z_{AN+}(V_{iN+} - V_{iN-})}
\]
\[
R_{out-} = R_L \frac{1 - \frac{V_{out-}}{Z_{AN-}(V_{iN+} - V_{iN-})}}{Z_{AN-}(V_{iN+} - V_{iN-})}
\]
REQUIRED EQUATIONS FOR MAKING MEASUREMENTS (CONT.)

The following equations are used to determine high frequency schematic values. Determination of pole frequencies must be made manually. The input frequency is swept, and the pole is determined to be the frequency at which the amplitude has dropped by a factor of $1/\sqrt{2}$. The output pole measurements must be made with a load capacitance that makes it the dominant pole so that frequency variations due to the input pole do not compromise the measurements. For the output capacitance, the average output resistance found in Eqs. (4) and (5) can be used. We will also use frequency measurements to verify the output resistance measurements.

\[
\begin{align*}
(C_{BP} + C_{inP+}) & = \frac{1}{2\pi \left( R_{inP+} / R_t \right) f_{iP+}} \\
(C_{BP} + C_{inP-}) & = \frac{1}{2\pi \left( R_{inP-} / R_t \right) f_{iP-}} \\
(C_{BP} + C_{inN+}) & = \frac{1}{2\pi \left( R_{inN+} / R_t \right) f_{iN+}} \\
(C_{BP} + C_{inN-}) & = \frac{1}{2\pi \left( R_{inN-} / R_t \right) f_{iN-}} \\
(C_{BP} + C_{in}) & = \frac{1}{2\pi \left( R_{in} / R_t \right) f_{in}}
\end{align*}
\]

\[
\begin{align*}
(C_{BP} + C_{out+}) & = \frac{1}{2\pi R_{out+} f_{out+}} - C_{L+} \\
(C_{BP} + C_{out-}) & = \frac{1}{2\pi R_{out-} f_{out-}} - C_{L-}
\end{align*}
\]

Using multiple load capacitance values also allows the determination of $R_{out}$. This must be done with a load capacitance which causes the dominant pole to be caused by the output node at a frequency much lower than the input pole frequency. This can be done to double check the output resistance calculation.

\[
\begin{align*}
R_{out+} & = \frac{1}{2\pi (C_{L1} - C_{L2})} \left( \frac{1}{f_{out+1}} - \frac{1}{f_{out+2}} \right) \\
R_{out-} & = \frac{1}{2\pi (C_{L1} - C_{L2})} \left( \frac{1}{f_{out-1}} - \frac{1}{f_{out-2}} \right)
\end{align*}
\]
NOISE CONSIDERATIONS

Difficulty in making precise measurements arises from the presence of noise. In an attempt to achieve good measurements, the signal-to-noise ratios (SNR) should be considered. The input SNR due to the Thevenin input resistance is:

\[ SNR_{R_t} = \frac{V_i^2}{KT (R_{in} + R_t)} (C_{BP} + C_{in}) \]

This indicates that the noise can be reduced by reducing the input bandwidth via increasing the input capacitance, or by reducing the Thevenin input resistance.

For an input SNR of \( \sim 200 \), the following values are required: \( V_i = 100mV \), \( I_{in} = 100nA \), \( R_t = 1M\Omega \), \( R_{in} \approx 50\Omega \), \( C_{BP} \approx 1.7pF > > C_{in} \)

The amount of added noise due to the amplifier can be calculated as follows:

\[ I_{n+} = \frac{V_{n+}^2}{R_{n+}} - 4KT \frac{R_i}{(R_{in} + R_t)^2} \pi f_{n+} \]
\[ I_{n-} = \frac{V_{n-}^2}{R_{n-}} - 4KT \frac{R_i}{(R_{in} + R_t)^2} \pi f_{n-} \]
\[ I_{n+} = \frac{V_{n+}^2}{R_{n+}} - 4KT \frac{R_i}{(R_{in} + R_t)^2} \pi f_{n+} \]
\[ I_{n-} = \frac{V_{n-}^2}{R_{n-}} - 4KT \frac{R_i}{(R_{in} + R_t)^2} \pi f_{n-} \]

MEASUREMENTS CONCERNS

The concern for making measurements is the input signal amplitude and the ability to measure the input node voltage. The amplifier requires very small input currents which produces very small input signal amplitudes that may be too small to measure with an oscilloscope. For example, if we use an input current of 100nA, with \( R_{in} \approx 50\Omega \) and \( R_{in} \approx 1K\Omega \), \( V_{in} \approx 5\muV \) and \( V_{in} \approx 100\muV \) respectively. The minimum measurable voltage on the oscilloscope is in the mV range.

It is recommended that instead of using an oscilloscope and arbitrary wave form generator, an RF signal generator and spectrum analyzer and network analyzer is used. Their capabilities of generating and measuring much smaller amplitudes (dBµV) may help.
Independent testing done by:

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