



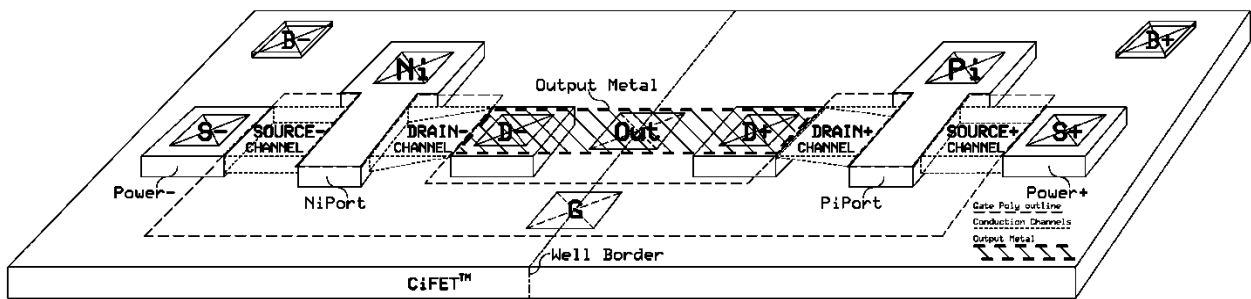
Seven Ways Circuit Seed's Circuit Designs Reduce Noise

In the end, it comes down to signal-to-noise ratio. Low power supply voltage requirements in ultra-deep-sub-micron (below 28nm) integrated circuit processes limit the maximum signal swing to a much smaller number than most analog designers are used to. So with a smaller signal, the noise must be equally small in order to maintain the desired signal to noise ratio. It is imperative that noise issues be reduced. The CiFET amplifier technology not only reduces noise by an amount that would be necessary but performs far beyond expectations, delivering ultra-quiet front ends.

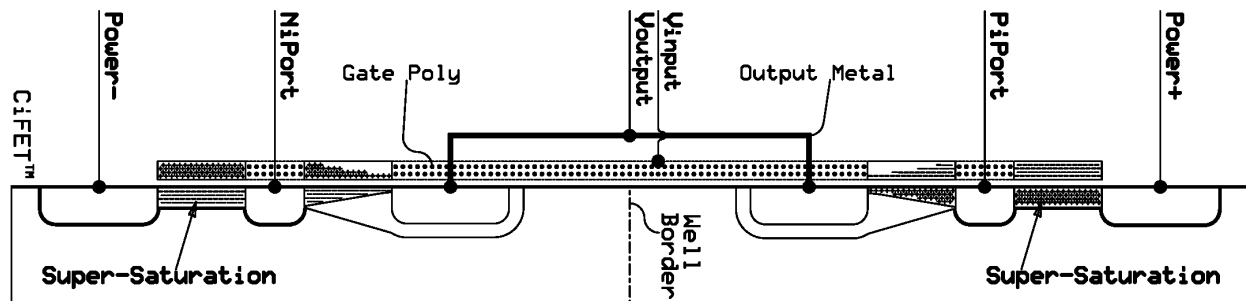
- 1. Source Channel.** $1/f$ noise in the source channel is reduced because the self-bias scheme provides a high field strength on the source channel's gate, forcing carriers in the channel to operate below the surface, where there is a smoother path (fewer obstructions), rather than along the surface where crystal lattice defects interfere.
- 2. Drain Channel.** $1/f$ noise in the drain channel is low. Unlike conventional analog designs, the gate is self-biased at the half-way point between the power supply rails, as is the drain, while the iPort is within ~ 100 millivolts of the power rail. With the high electric field along the drain channel, and the gate voltage equal to the drain terminal voltage, the carriers are constrained to flow mostly below the channel surface. This keeps the drain channel out of pinched off conditions, where unwanted $1/f$ noise would be generated.
- 3. Resistor Noise.** Resistor noise is reduced because the self-bias configuration puts the complementary pair at its lowest channel resistance operating point. Resistance is caused by collisions between carriers and the surrounding atoms in the conductor. The lower the resistance, the fewer the collisions.
- 4. Wide Band Noise.** Wide band noise (white-noise) is always an issue in high gain, high frequency circuits. While conventional designs adjust the gate voltage to establish the operating point, Circuit Seed designs establish the gate voltage at the optimum point (the "sweet-spot") and then adjust the load to establish the desired operating point. This approach establishes a higher quiescent current where, for reasons explained above, higher current density circuits have lower wide band noise.
- 5. Power Supply Noise.** High common mode power supply rejection is inherent in the complementary CiFET circuit. Signals are with respect to the mid-point instead of being with respect to one of the power supply rails (similar to an op amp with its "virtual" ground). Power supply noise is from one rail to the other, equal and opposite in phase with respect to each other, thus canceling around the mid-point.
- 6. Ground-Loop noise** is diminished because the circuit ground is "virtual" (just like in many op-amp circuits) rather than ground being one or the other power supply connections. In the

closed-loop case, “flying capacitors” are employed. With “flying capacitors” there is no direct electrical connection between stages, so there is no common ground, virtual or otherwise. The use of “differential decoupling” (flying capacitors) offers transformer-like isolation between stages with the compactness of integrated circuit elements.

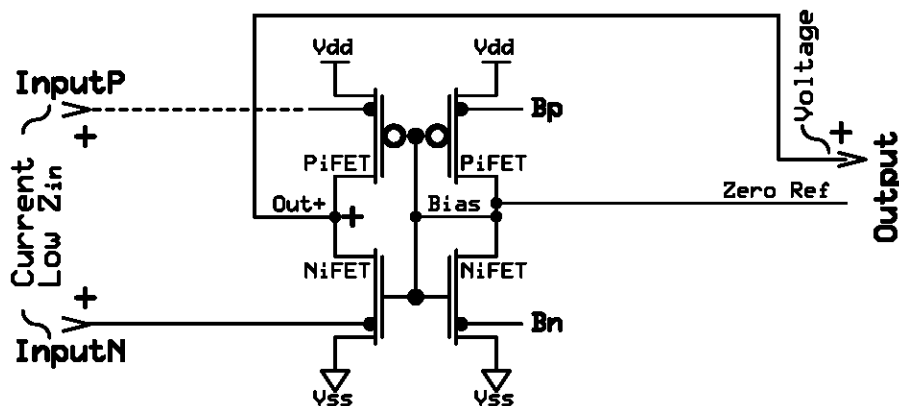
7. **Coupled noise** from “parasitic induced crosstalk” increases by the square of the signal amplitude. Unintended capacitive coupling with a 1 volt signal causes a lot more trouble than with a 100 mV signal, by a factor of 100:1 (square law effect). The small voltage signals employed in the analog sections reduce this capacitive coupled interference substantially. Nearby digital signals will, by definition, be high amplitude (rail-to-rail). Good layout practices are still the best defense against this digital source of noise.



Charge Based Complimentary iFET (CiFET)



Cross Section View



Biased single-stage CiFET Transresistance amplifier