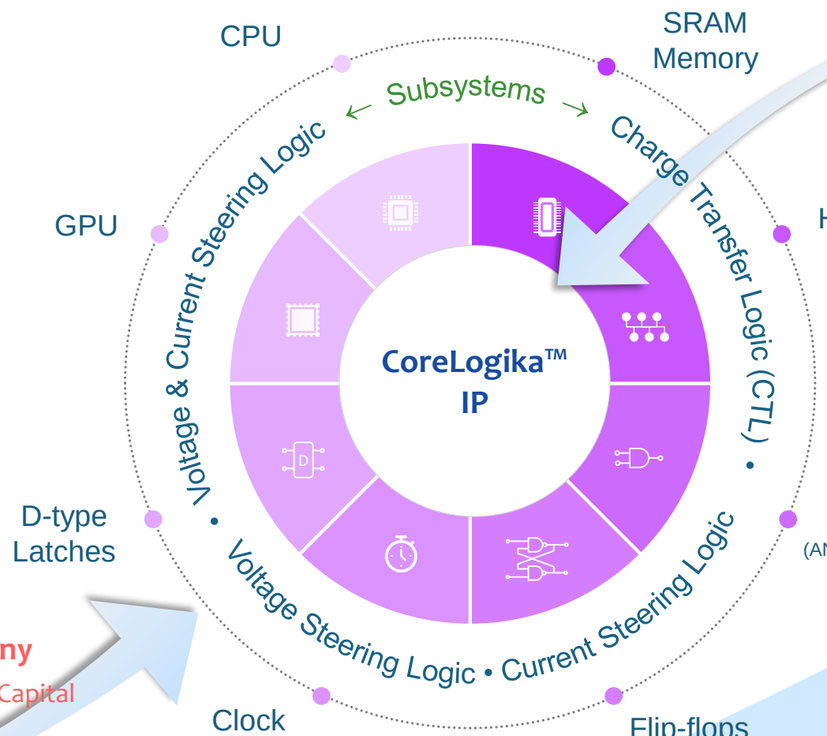
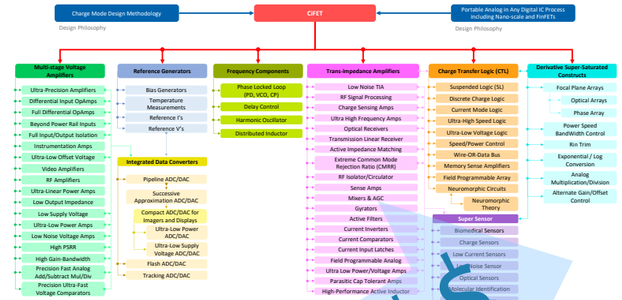
CoreLogika™

Hyper Speed Logic Computing

- Speed 10 – 100 Times Faster
- Combination of Low Power & High Speed
- Temperature Beyond Military Specs
- Tolerant to Parametric Variation
- Modulation of Inputs
- Multi $B Markets
- Intuitive



Circuit Seed IP Portfolio Advantage



CTL Published Patent
WO2019183174A1

X Operating Company

- Requires too Much Capital
- Takes too Long
- Frequently Pivoting
- Unnecessary Business Risk
- High Market Adoption Risk
- Massive Dilution
- Low Probability of Success

✓ SPJV Invention Company (Fabless)

- Partnering with Global Companies
- Lower Capital Requirements
- Extremely Compressed Timeline
- Outsources Business Execution & Manufacturing Risk
- No Market Adoption Risk
- Minimal Dilution
- Higher Revenue Participation

Financial Returns $ $ $ $ $

Social Impact Returns ☺☺☺☺☺

"Amplify & Leverage" the Invention Portfolio

Disciplined Competitive Analysis

Set Scope for Product Initiatives (High Performance Computing) (IP Amplification)

Create POC Near Market Solution Circuits "On Demand" Feature Sets

Usual Suspects (Intel, AMD, Nvidia, Qualcomm, ARM, Apple, IBM, Samsung)

Unusual Suspects (Microsoft, Alphabet, Amazon, TSMC, Cadence, Synopsis)

Universities, Gov't Labs, Foundations

New Emerging Technology Invention Companies

In Parallel for Speed

OEM Product

—

"New Business Models"

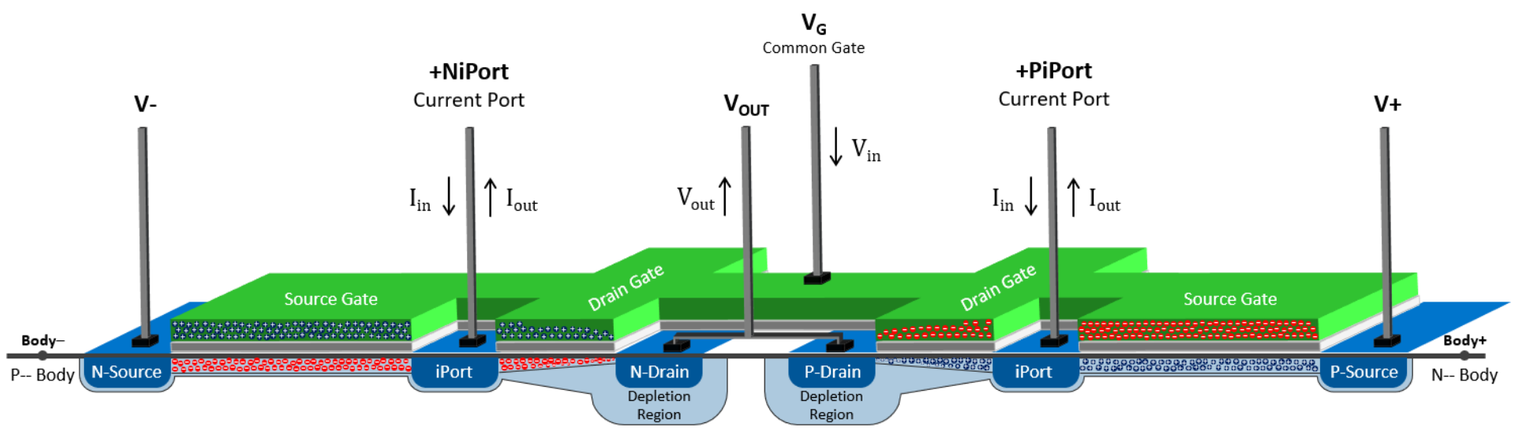
Global Adoption

—

Early M&A Partnership Public Offering

CoreLogika™

CiFET any Number of Input AND/OR/Inverter Logic Gate



CTL is a new approach to performance and enhanced capabilities of digital logic at less cost.

Improvements in various combinations of less power consumption, higher speed (10 to 100 times), smaller footprint and less heat

- Combined digital and analog functionality (0,1,"n"), n = graded logic
- Conventional digital modes (0,1) plus "NO-Change" status where no current or voltage flows
- Voltage steering logic, Current steering logic, combination
- Tolerant to parametric variation
- Wide temperature range beyond military specifications
- Predictable heat generation over a wide range of frequencies

InventionShare is seeking investment partners with significant digital logic experience to develop CoreLogika designs, building the libraries and test circuits in silicon. Similar CMOS CiFET analog circuits designs are already fabricated and tested showing excellent results with no changes in manufacturing.